This listing of claims replaces all prior versions, and listings of claims in the instant application:

Listing of Claims:

1. (Cancelled) Please Cancel Claim 1, without prejudice.

2. (Cancelled) Please Cancel Claim 2, without prejudice.

3. (Cancelled) Please Cancel Claim 3, without prejudice.

4. (Currently Amended) The ~~boosted memory array of Claim 2,~~ A boosted memory array comprising:

at least one bitline;

at least one memory cell coupled to said bitline;

a bitline booster circuit coupled to said bitline;

a bitline booster circuit bitline boost enable signal input terminal coupled to said bitline booster circuit;

a bitline boost enable signal coupled to said bitline booster circuit bitline boost enable signal input terminal, wherein;

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when said bitline boost enable signal is active and a signal on said at least one bitline starts going low, said bitline booster circuit discharges said at least one bitline, further wherein;

said boosted memory array includes at least two bitlines, a first bitline and a second bitline, further wherein;

said bitline booster circuit comprises:

a first NOR gate, a first input of said first NOR gate being coupled to said first bitline and a second input of said first NOR gate being coupled to said bitline boost enable signal;

a first transistor, an output of said first NOR gate being coupled to a control electrode of said first transistor, a first flow electrode of said first transistor being coupled said first bitline, a second flow electrode of said first transistor being coupled to a supply voltage;

a second NOR gate, a second input of said second NOR gate being coupled to said second bitline and a second input of said second NOR gate being coupled to said bitline boost enable signal; and

a second transistor, an output of said second NOR gate being coupled to a control electrode of said second transistor, a first flow electrode of said second transistor being coupled said second bitline, a second flow electrode of said second transistor being coupled to said supply voltage.

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5. (Original) The boosted memory array of Claim 4, wherein;

said first and second transistors are NFETS and said supply voltage is ground.

6. (Original) The boosted memory array of Claim 4, wherein;

said boosted memory array is on the same silicon chip as a microprocessor.

7. (Cancelled) Please Cancel Claim 7, without prejudice.

8. (Cancelled) Please Cancel Claim 8, without prejudice.

9. (Cancelled) Please Cancel Claim 9, without prejudice.

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10. (Currently Amended) ~~The microprocessor chip of Claim 9,~~ A microprocessor chip, said microprocessor chip comprising:

one or more functional blocks; and

a boosted memory array, said boosted memory array comprising:

at least one bitline;

at least one memory cell coupled to said bitline;

a bitline booster circuit coupled to said bitline;

a bitline booster circuit bitline boost enable signal input terminal coupled to said bitline booster circuit;

a bitline boost enable signal coupled to said bitline booster circuit bitline boost enable signal input terminal, wherein;

when said bitline boost enable signal is active and a signal on said at least one bitline starts going low, said bitline booster circuit discharges said at least one bitline, further wherein:

said boosted memory array includes at least two bitlines, a first bitline and a second bitline, further wherein;

said bitline boost enable signal is active only during write operation, further wherein;

said bitline booster circuit comprises:

a first NOR gate, a first input of said first NOR gate being coupled to said first bitline and a second input of said

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first NOR gate being coupled to said bitline boost enable signal;

a first transistor, an output of said first NOR gate being coupled to a control electrode of said first transistor, a first flow electrode of said first transistor being coupled said first bitline, a second flow electrode of said first transistor being coupled to a supply voltage;

a second NOR gate, a first input of said second NOR gate being coupled to said second bitline and a second input of said second NOR gate being coupled to said bitline boost enable signal; and

a second transistor, an output of said second NOR gate being coupled to a control electrode of said second transistor, a first flow electrode of said second transistor being coupled said second bitline, a second flow electrode of said second transistor being coupled to said supply voltage.

11. (Original) The microprocessor chip of Claim 10, wherein;

said first and second transistors are NFETS and said supply voltage is ground.

12. (Cancelled) Please Cancel Claim 12, without prejudice.

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13. (Cancelled) Please Cancel Claim 13, without prejudice.

14. (Cancelled) Please Cancel Claim 14, without prejudice.

15. (Currently Amended) ~~The method for boosting the performance of a memory array of Claim 14,~~ A method for boosting the performance of a memory array comprising:

providing at least one bitline;

coupling at least one memory cell to said at least one bitline;

coupling a bitline booster circuit to said at least one bitline;

coupling a bitline booster circuit bitline boost enable signal input terminal to said bitline booster circuit;

coupling a bitline boost enable signal to said bitline booster circuit bitline boost enable signal input terminal, such that;

when said bitline boost enable signal is active and a signal on said at least one bitline starts going low, said

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bitline booster circuit discharges said at least one bitline, wherein;

said boosted memory array includes at least two bitlines, a first bitline and a second bitline, further wherein;

said bitline boost enable signal is active only during write operation, further wherein;

said bitline booster circuit comprises:

a first NOR gate, a first input of said first NOR gate being coupled to said first bitline and a second input of said first NOR gate being coupled to said bitline boost enable signal;

a first transistor, an output of said first NOR gate being coupled to a control electrode of said first transistor, a first flow electrode of said first transistor being coupled said first bitline, a second flow electrode of said first transistor being coupled to a supply voltage;

a second NOR gate, a first input of said second NOR gate being coupled to said second bitline and a second input of said second NOR gate being coupled to said bitline boost enable signal; and

a second transistor, an output of said second NOR gate being coupled to a control electrode of said second transistor, a first flow electrode of said second transistor being coupled said second bitline, a second flow electrode of said second transistor being coupled to said supply voltage.

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16. (Original) The method for boosting the performance of a memory array of Claim 15, wherein;

said first and second transistors are NFETS and said supply voltage is ground.

17. (Original) The method for boosting the performance of a memory array of Claim 15, wherein;

said boosted memory array is on the same silicon chip as a microprocessor.

18. (Cancelled) Please Cancel Claim 18, without prejudice.

19. (Cancelled) Please Cancel Claim 19, without prejudice.

20. (Cancelled) Please Cancel Claim 20, without prejudice.

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21. (Currently Amended) ~~The method for improving the performance of a microprocessor chip of Claim 20,~~ A method for improving the performance of a microprocessor chip, said method comprising:

providing one or more functional blocks on said microprocessor chip;

providing a boosted memory array, said boosted memory array comprising:

at least one bitline;

at least one memory cell coupled to said bitline;

a bitline booster circuit coupled to said bitline;

a bitline booster circuit bitline boost enable signal input terminal coupled to said bitline booster circuit;

a bitline boost enable signal coupled to said bitline booster circuit bitline boost enable signal input terminal, wherein;

when said bitline boost enable signal is active and a signal on said at least one bitline starts going low, said bitline booster circuit discharges said at least one bitline, further wherein;

said bitline boost enable signal is active only during write operation, further wherein;

said bitline booster circuit comprises:

a first NOR gate, a first input of said first NOR gate being coupled to said first bitline and a second input of said

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first NOR gate being coupled to said bitline boost enable signal;

a first transistor, an output of said first NOR gate being coupled to a control electrode of said first transistor, a first flow electrode of said first transistor being coupled said first bitline, a second flow electrode of said first transistor being coupled to a supply voltage;

a second NOR gate, a first input of said second NOR gate being coupled to said second bitline and a second input of said second NOR gate being coupled to said bitline boost enable signal; and

a second transistor, an output of said second NOR gate being coupled to a control electrode of said second transistor, a first flow electrode of said second transistor being coupled said second bitline, a second flow electrode of said second transistor being coupled to said supply voltage.

22. (Original) The method for improving the performance of a microprocessor chip of Claim 21, wherein;
said first and second transistors are NFETS and said supply voltage is ground.

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